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TITLE: CHIP LEAD FRAMES

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Application for United States Patent

in the name of Takashi Kumamoto (Kouyadai, Japan),

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CHIP LEAD FRAMES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 USC is a continuation-in-part of U.S. Patent Application Serial No. 09/741,535, filed on December 29, 2000, the entire contents of which are hereby incorporated by reference.

BACKGROUND

This invention relates to chip lead frames.

A semiconductor chip can include millions of transistor circuits, each smaller than a micron, and multiple connections between the chip and external elements.

Referring to Figure 1A, a so-called flip chip configuration facilitates a compact assembly, reduced footprint size on boards, and shorter and more numerous input-output (I/O) connections with improved electrical and thermal performance. A flip chip typically includes a die 101 with solder bumps 110 that are interconnected conductive elements to a substrate 114.

One method of electrically connecting a flip chip utilizes controlled-collapse chip connection technology (C4). First, solder bumps 110 are applied to pads on the active side of the die 101, the substrate 114 or both. Next, the solder bumps 110 are melted and permitted to flow, ensuring that the bumps are fully wetted to the corresponding pads on the die 101 or substrate 114. A tacky flux is typically applied to one or both of the surfaces to be joined. The flux-bearing surfaces of the die 101 and substrate 114 are then place in contact with each other in general alignment. A reflow is performed by heating the die 101 and substrate package to or above the solder's melting point. The solder on the chip and the substrate combine and the surface tension of the molten solder causes the corresponding pads to self-align with each other.

The joined package is then cooled to solidify the solder. The resulting height of the solder interconnects is determined based on a balance between the surface tension of the molten solder columns and the weight of the chip. Any flux or flux residue is removed from the die 101 and substrate 114 combination in a defluxing operation.

Finally, an epoxy underfill 116 is applied between the bottom surface of the die 101 and the top surface of the substrate 114, surrounding and supporting the solder columns. The reliability and fatigue resistance of the die-substrate solder connection is increased significantly. The underfill 116 acts to carry a significant portion of the thermal loads

induced by coefficient of thermal expansion (CTE) differences between the chip and substrate, rather than having all the thermal load transferred through the solder columns. The underfill 116 can also electrically insulate the solder columns from one another.

For some integrated circuit applications, it is desirable to utilize as thin a substrate or film as possible to maximize the electrical performance of the resulting packaged chip. Typically, thin substrates or films include a polymeric material and are 0.05 to 0.5 mm thick. A thin substrate's shorter vias help reduce loop inductance within the substrate. These thin substrates are very flexible and can cause difficulties for attaching solder balls or pins. In unreinforced form they are susceptible to damage during installation and removal operation. One current practice is to bond rigid blocks 111 of a suitable material to the periphery of the substrate using an adhesive layer 112.

The attached rigid block 111 stiffens the entire package. Referring also to Figure 1B, support bars 109 from the rigid block 111 can be used to strengthen individual elements, such as a land grid array (LGA) pad 230 that is attached to a flip chip pad 206 by a routing lead 204.

It is also known to run the epoxy adhesive up the sides of the die 101 to form an epoxy fillet that reinforces the die (see, e.g., U.S. Patent No. 6,049,124).

DESCRIPTION OF DRAWINGS

Figures 1A and 1B are schematics of a conventional flip chip configuration.

Figure 2 is a schematic of a first process of packaging a die 101 and substrate 105.

Figure 3 is a sequence of cross sections and schematics for a second process of packaging a die 101 and substrate 105.

Figure 4 is a schematic of a process of packaging dies 101. The process includes dicing the substrate 105.

Figure 5 is a flow chart for a process of packaging a die 101.

Figure 6 is a schematic of a process of packaging a die using a half-etched lead frame 105

Figure 7 is a schematic of a routing lead and pad.

Figure 8 is a schematic of a ball grid array.

DETAILED DESCRIPTION

Referring to the example in Figures 2A to 2G, a die 101 is attached to a substrate 105, and then packaged to form an assembly 160 (figure 2G).

Referring to Figure 2A, the die 101 is first oriented with respect to the substrate 105. The die 101 can be a chip or silicon wafer that bears an integrated circuit. The substrate 105 can be a conductive material such as copper. For example, the substrate 105 can be a continuous copper, or other conductive, foil. The copper foil can include at least about 40%, 50%, 70%, 90%, or 99% copper by weight. The low

electrical resistance of copper improves the performance of the fabricated flip chip assembly.

The substrate can be less than about 22, 20, 18, or 16 μm thick.

The substrate 105 can have insulative pads 108 for mounting passive components 103 such as decoupling capacitors that lower the power supply loop inductance.

The die 101 includes solder bumps 110 for forming interconnects with the substrate 105. Examples of solder compositions include high temperature bump (e.g., 97% Pb and 3% Sn), eutectic bump (63% Pb and 37% Sn), stud bump (e.g., 100% Au), and conductive epoxies. Bumps can be formed by combinations of the above, for example, as a high temperature bump which is plated with a eutectic bump.

The bumps 110 can be arranged in a regular array on the die lower surface. For example, the bumps can have a pitch of about 11 mils (279.4 μm).

Referring to Figure 2B and also to Figure 6, the die 101 is disposed 610 on the substrate 105 such that the bumps 110 contact the substrate. Heat is used to attach 620 the solder bumps 110 to the substrate 105.

In some embodiments, thermo-compression bonding is used to locally heat the die 101 with a pulse of heat. For example, the bonding process can apply 2 gf / bump and a heat pulse of 230°C for 3 second. Such a process can obviate the

need for a flip chip pad that has solder resist dams positioned to receive the solder bumps 110.

In other embodiments, a reflow furnace is used to melt the solder bumps and bond them to the substrate 105. The substrate can include solder resist dams to contain the reflowing solder of each bump. See below for a description of the use of an interposer layer 300 to form solder resist dams.

After attachment of the die, the die 101 lower surface and the substrate upper surface form a gap 115 which is spanned by contacts formed from the solder bumps 110. The gap can, for example, be less than about 120, 100, 80, or 50 μm.

Referring to Figures 2C and 2D, the substrate 105 is placed 630 between a bottom mold 120 and a top mold 130. The mold top 130 and/or bottom 120 can include any suitable material, including various metals, plastics, ceramics, and composites. The mold can have sufficient rigidity that it retains its form while a composition is being injected into the mold cavity 145 under pressure.

The top mold 130 can bear a release film 125. The release film 125 can be a heat resistive film that separates the die 101 upper surface 102 from the top mold 130. The release film 125 can be used to prevent flashes to the die 101 upper surface 102 in order to maintain the upper surface 102 free of the epoxy. One exemplary release film is provide by Film Assisted Molding Equipment (Fame®) from Apic Yamada Corp.,

Japan. The release film can include fluorocarbon-based polymers and have a thickness of 0.5 to 5 mils.

The mold can include small air vents, e.g., opposite the runner 140, to allow air to escape from the cavity 145 when displaced by the injected composition.

Referring to Figure 2E, a composition which can form a polymer is injected 640 into the runner 140 that connects to the mold cavity 145. The composition can be delivered under pressure, e.g., in a hot plastic state from an auxiliary chamber through runners and gates into the cavity 145. After injection, the composition can be allowed to set and form a polymer network 150 that extends between the cavity between the die 101 and the substrate 105. The setting process can include incubation under curing conditions.

By forming a polymer network that underfills the die 101 and extends to all regions of the substrate that are not covered by the die or another component (such as the passive components 103), the assembly 160 is rigidified and strengthened, even though it lacks a rigid support member (such as the rigid frame 111).

The extent of the polymer network can be varied, for example, by appropriate mold (120 and 130) design. Accordingly, in some embodiments, the polymer network can form layers of varying heights (i.e., in a direction normal to the substrate 105), e.g., up to the lower die surface, to the upper die surface, or 205, 40%, 50%, 60%, or 80% between the two.

Similarly, the extent of the polymer network along the plane of the substrate 105 can vary, again, by appropriate mold design. Accordingly, in some embodiments, the polymer network extends at least to a passive component 103 or other component attached to the substrate 105, to another die 101 disposed on the same substrate 105, or to the perimeter of the substrate 105. The polymer network can (additionally or alternatively) extends a distance (parallel to plane of the substrate 105) away from the die perimeter that is at least the height of the die 101, i.e. the distance from the die lower surface that opposes the substrate 105 to the die upper surface.

A variety of compositions can be used to form the underfill and rigidified assembly. The compound can be a resin, or another compound that forms a polymer. The polymer is typically non-conductive. A continuous rigid network is the contiguous structure formed by setting the compound. The structure imparts rigidity to the substrate 105 (or lead frame 210, as described below).

Resins include crystalline resins, and multi-functional-type resins. Other resins, such as BMI's, polyesters, and thermoplastics, may be utilized as appropriate.

In some embodiments, the compound is an epoxy, such as glass-filled epoxy. The epoxy resin utilized can have high strength and good thermal properties, including resistance to the high temperatures that can be generated by an integrated chip during operation. Additionally, epoxy in the uncured

liquid state can have relatively low viscosities to facilitate injection into the space between the chip and substrate surfaces. For example, the epoxy can have a melt viscosity of less than about 20, 15, 12, 10, or 8 Pa·s at 165°C.

Table 1 lists some of the properties of an exemplary epoxy formulation. Such properties are non-limiting and may be present alone or in combinations with other properties.

In general, the difference in the coefficient of thermal expansion (CTE) between virgin unfilled epoxy and either a silicon chip or a reinforced plastic substrate will be significant. Given the wide range of operating temperatures that a flip chip package may experience, it is desirable to tailor the CTE's of the joined materials to be as close as possible, thereby minimizing any induced thermal stresses. Conversely, too much filler could cause the viscosity of the epoxy formulation to increase to a point where it is resistant to flow in the gap between the top of the chip 110 and the corresponding surface of the substrate 120. Additionally, if the filler has a higher modulus than the virgin epoxy, it acts to increase the stiffness of the cured epoxy formulation, which results in greater rigidity for the resulting chip package. Accordingly, a filled epoxy resin comprising about 80% by weight silica microspheres is believed to be the ideal formulation.

Table 1

Filler material	Silica
Filler shape	All Spherical
Filler content	80 wt%
Mean particle size	4μm
Maximum particle size	12μm
Curing condition	165°C/120sec
Spiral flow	180°cm at 165°C/120sec, 6.9N/mm2
Gelation time	30sec at 165°C
Hot hardness	85 at 165°C/120 sec
Melt viscosity	10Pas at 165°C
Glass transition temperature	145°C
CTE below Tg	14ppm
CTE above Tg	56ppm
Specific gravity	1.88 at 25°C
Thermal conductivity	0.63 W/m*C
Flexural modulus	13700 N/mm^2 at 25°C
Flexural strength	120 N/mm^2 at 25°C
Volume resistivity	1.00E+14 ohm*m 25°C
Water absorption	0.5%

It is also desirable to have an epoxy formulation that cures relatively quickly at an elevated temperature so that ship packages can be fabricated at production rates, but that has a relatively long pot life at room temperature or even slightly elevated temperatures so that the mixed epoxy and catalyst does not cure in the supply lines before being injected into the mold. The preferred resin has a cure profile of approximately 120 seconds at 165°C. Depending on the properties of an alternative resin formulation, different cure profiles may be specified that provide suitable results. It is also contemplated that certain thermoplastic resins may be utilized in the molding operation that do not have a cure

temperature but rather melt at an elevated temperature and solidly when cooled.

Utilizing an epoxy resin of the type and formulation specified in Table 1, the molding process would proceed as follows. First, the mold is either heated to 165°C with the incomplete chip package contained therein, or the mold is maintained at 165°C and the incomplete package is inserted therein. Next, the epoxy resin is injected through runner 140 in the mold at a pressure or around 1-5 MPa. The resin may be preheated to an intermediate temperature to lower the viscosity of the resin and facilitate the resin transfer modeling process. Once the proper amount of epoxy is injected into the mold cavity, the mold is held at 165°C for at least 120 seconds to fully cure the epoxy.

Referring to Figures 2F and 6, after cure, the mold is separated and the assembly 160, as depicted in Figure 2F, is removed 650. Typically, the molded flip chip package will be removed while the mold is hot so that the mold may immediate be re-used to fabricate another package; however it is conceivable that the mold may be permitted to cure before removing the molded flip.

Referring to Figure 2G, the assembly 160 is trimmed to provide an epoxy-surrounded and underfilled die 101 on the conductive substrate 105.

Referring to Figures 3A to 3E, a variation of the above process is used for fabrication of the flip chip-substrate

assembly 160. A thin substrate 105 is coated with a insulative resist layer 300. The insulative layer is etched or otherwise modified to excise regions 310 that can accept solder balls or other contacts from components. The insulative layer 300 has high electrical resistance, i.e., it is formed from a non-conductive material.

Referring also to Figure 3B, a die 101 is placed on the substrate 105 such that the solder balls 110 on the die 101 are positioned in the excised acceptor regions 310. When appropriately heated the solder balls reflow and form stable electrical contacts with the substrate 105. Similarly passive components 103, such as a capacitor, are also connected to the substrate by solder contacts 112.

Referring to Figure 3C, as described above, the assembly formed by the die 101, passive components 103 and substrate 105 are surrounded in a mold and coated 640 with an epoxy layer 150 that forms a continuous rigid supporting structure 150.

If a gap is formed between the insulative layer 300 and the die 101 lower surface, then the structure formed by the epoxy layer can fill the gap.

After forming the epoxy casing 150 as depicted in both Figures 2G and 3D, the conductive substrate 105 is modified by etching 660 to fabricate a lead frame 210. Etching 660 is not limited to chemical etching. For example, the etching 660 can be done by UV- or CO_2-high powered laser abrasion, photolithographic, or traditional copper etching processes.

Referring to Figure 3, the etching 660 leaves conductive paths 204 that connect, for example, each die interconnect 110 with a terminus 230.

The termini 230 can be arranged for convenient interfacing with any of a variety of chip interface formats, such as land grid arrays (LGA), ball grid arrays (BGA), pin grid arrays (PGA), printed circuit boards (PCB), or mother boards.

Referring to Figure 7, the rigidity and support provided by the epoxy encasement 150 not only allows the use of thin substrates 105, but also high density of C4 pads 206 and routing leads 204. For example, the center to center distance 582 between two C4 pads 206 can be less than about 0.127 mm, e.g., about .12, .10, .09, .08, .083, .07 mm or less. In other words, the pitch 581 between a first C4 pad and a fourth adjacent C4 pad is less than about 0.35, 0.3, 0.27, 0.25, or 0.2 mm.

Subsequently, an insulative coating 370 is applied 670 to the etched substrate. The insulative compound can be the same or different from the epoxy compound used to form the epoxy casing and underfill. The insulative compound forms a resist coat 370 that guards against shorts between different conductive paths 204 of the lead frame formed from the substrate 105.

In another implementation, as depicted in Figure 6A, a half-etched substrate 705 is used. For a substrate having a thickness of about 18 μm, half-etches 710 are created that are

about 9 μm deep and that are backed by an underlayer 730 of the substrate 705. Referring to Figure 6B, the die 101 is disposed on the half-etched substrate 705 such that the die bumps 110 form interconnects along ridges 720 of the half-etched substrate 705. Referring to Figure 6C, the assembly is contacted with the polymer composition to form a network 150 that rigidifies and strengthens the assembly. Referring to Figure 6D, the bottom half or substrate underlayer 730 of the half-etched substrate 705 is then removed in order to fabricate the lead frame 210.

The steps 610 to 670 can be performed for multiple dies 101 in parallel, for example, as depicted in Figure 5. Referring to Figure 5A, multiple dies 101 are disposed on a panel that consists of the substrate 105. Reels, strips, and other formats of the substrate 105 can also be used.

Referring to Figure 5B, the entire assembly is placed in the molds and encapsulated with epoxy to form the rigidified assembly 410. The lower surface of the substrate 105 can then be etched 660 to generate a lead frame. The etching can include exposing a display area 420 on the substrate lower surface 430 to light projected through a photolithographic mask.

Referring to Figure 5C and also to Figure 6, the substrate 105 is diced 680 to separate individual devices 450 that include a die 101 and its lead frame 210. Typically, after dicing, each individual device includes an encapsulating

layer that extends to the perimeter of the device, i.e. of the lead frame 210.

The techniques described here are not limited to the examples described above.

For example, the gap 115 can be filled with underfill prior to placement of the die 110 in the molds using the same composition or a different composition from the composition used to form the encapsulating network 150. By adjusting the shape of the molds, the encapsulating network 150 can be fabricated in a variety of configurations, e.g., extending at least to the lower die surface, at least to the upper die surface, or at least 25%, 50%, 75%, or 90% of the distance to the upper die surface from the lower die surface. In still another example, the encapsulating network 150 covers the upper die surface, as depicted in Figure 8.

As described above, a lead frame produced by a method described here can be used in a variety of interface formats. Referring to Figure 8, the lead frame 210 is connected to a BGA that includes multiple solder bumps 830 spaced with a pitch 840 of about 1 mm. The lead frame 210 can also include additional features such as a gold wire 810 that connects to the die 101. The assembly is encased in a polymer composition that covers the die upper surface 102, thus, forming an additional encapsulating layer 150. The assembly can have a height 820 of about 1.2 mm.

As depicted in Figure 8, the gap between the lead frame 210 and the balls 830 is filled with an underfill composition

850 that differs from the encapsulating layer 150. The insulative coat 220 forms a resistive layer between the lead frame 210 and the solder balls 830.

Other implementations are within the scope of the claims.